UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/818,766	03/27/2001	Masakazu Taguchi	0941.65368	2399

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EXAMINER
RODRIGUEZ, GLENDA P

ART UNIT	PAPER NUMBER
2697	2

DATE MAILED: 05/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

Office Action Summary	Application No.	Applicant(s)
	09/818,766	TAGUCHI ET AL.
	Examiner	Art Unit
	Glenda P. Rodriguez	2697

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☐ Responsive to communication(s) filed on _____ .

2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-17* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1,2 and 6-11* is/are rejected.

7) ☒ Claim(s) *3-5 and 12-17* is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

    If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☒ All   b)☐ Some *   c)☐ None of:

       1.☐ Certified copies of the priority documents have been received.

       2.☐ Certified copies of the priority documents have been received in Application No. _____ .

       3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

    a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)   4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)   5) ☐ Notice of Informal Patent Application (PTO-152)

3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .   6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claim 15 is objected to because of the following informalities: Claim 15 is a dependent Claim that depends on Claim 15. Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada et al. (U.S. Pat. No. 5, 056, 116) in view of Byrne et al. (U.S. Pat. No. 6, 487, 672). Shimada et al. disclose an apparatus for reading recorded data, said apparatus comprising:

A sampling part sampling a read signal from recorded data of a recording medium by synchronizing with a first clock signal (Col. 4, Lines 52-57);

A first storing part consecutively storing a sample value obtained by said sampling part (See Fig. 22. Shimada et al. disclose that the analog to digital converter (Element 1) supplies the sampled signal to a buffer (Element 15), which is a storing part);

A data detecting part retrieving the sample value from said first storing part by synchronizing a second clock signal different from the first clock signal and detecting data by processing the sample value in accordance with a predetermined algorithm, so that the recorded data is read based on the data detected by said data detecting part (Col, 19, Lines 16-22 and Lines 30-40; See also Fig. 26. Shimada et al. teach that the Viterbi detector hold the sample for two periods of CLK1, deriving a new clock signal, CLK2, making the detector have a different clock signal than the analog to digital controller.).

Shimada et al. does also disclose that the data detecting part is synchronized with a second clock signal (Col, 19, Lines 16-22 and Lines 30-40; See also Fig. 26. Shimada et al. teach that the Viterbi detector hold the sample for two periods of CLK1, deriving a new clock signal, CLK2, making the detector have a different clock signal than the analog to digital controller.). Shimada et al. fail to disclose that the detector retrieves the sample from the first storing means. However, this feature is well known in the art as disclosed by Byrne et al., wherein it teach a analog to digital converter coupled to a buffer (a memory storage device) and the buffer coupled to a detector (See Fig. 1, Elements 6, 20, 22). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Shimada et al.'s invention in order for the detector to be after the memory because both

elements work at different clocking signals, it is able to control the flow of information being processed by the storage device.

4. Claim 2 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada et al. (U.S. Pat. No. 5, 056, 116) and Byrne et al. (U. S. Pat. No. 6, 487, 672)as applied to claim 1 above, and further in view of Leung et al. (U.S. Pat. No. 6, 546, 518).

Regarding Claim 2, Shimada et al. disclose all the limitations of Claim 1. Shimada et al. fail to disclose that the apparatus data detecting part comprises a recursive process conducing part conducting a recursive process for the sample data retrieved from the first storing part in accordance with the predetermined algorithm so that maximum likelihood data is detected. However, this feature is known in the art as disclosed by Leung et al., wherein it teach a Viterbi detector that uses maximum likelihood data detection (Col. 1, Lines 35-44). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Shimada et al.'s invention in order for the detector to perform maximum likelihood detection of the data in order to improve the efficiency when performing data detection.

Regarding Claim 8, Shimada et al. and Leung et al. disclose all the limitations of Claim 2. Shimada et al. and Leung et al. fail to disclose recursive process conduction part conducts said recursive process based on an iterative number, which number is defined so that a required time required completing said recursive process conducted does not exceed a scanning time required scanning a gap

provided between an address part recording an address of data and a data part recording the data. It is obvious to a person of ordinary skill in the art to know that the process takes a certain amount of time and also that a detector is able to perform recursive processes (in other words, performs detections over and over again) when processing a signal.

5. Claim 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada et al. (U.S. Pat. No. 5, 056, 116) and Byrne et al. (U. S. Pat. No. 6, 487, 672) as applied to claim 1 above, and further in view of Bushy, Jr. (U.S. Pat. No. 4, 896, 337). Shimada et al. and Byrne et al. disclose all the limitations of Claim 1. Shimada et al. fail to teach an apparatus comprising:

A second storing part consecutively storing a sample value obtained by said sampling part;

A first switching part switching to one of said first storing part and said second storing part; a second switching part switching to another one of said first storing part and said second storing part, which is not witched to by said first switching part;

Whereby one of said first storing part and said second storing part, which is switched to by said first switching part, stores the sample value, while said data detecting part retrieves the sample value from another one of said

first storing part and said second storing part, which is switched to by said second switching part.

However, this feature is well known in the art as disclosed by Bushy, Jr., wherein it teaches an apparatus that has two different memory devices that receive the data and a switch between both memory devices (Pat. No. 4, 896, 337; See Fig. 3, Elements 30, 33, 41 and 42). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Shimada et al.'s invention in order for the medium to have more than one memory device in order to control more efficiently the manipulation of data.

Regarding Claims 10 and 11, Shimada et al., Byrne et al. and Bushy, Jr. disclose all the limitations of Claim 9. Shimada et al., Byrne et al. and Bushy, Jr. fail to disclose data detecting part comprises a recursive process conducting part conducting a recursive process for the sample value, which is retrieved from one of said first storing part and said second storing part, which is switched by said second switching part, in accordance with the predetermined algorithm, and detecting the maximum likelihood data, by synchronizing with said second clock signal. It would have been obvious to a person of ordinary skill in the art, to combine two memory devices connected by a switch (Pat. No. 4, 896, 337; See Fig. 3, Elements 30, 33, 41 and 42) to be detected and processed by a detector (it is known that a detector performs recursive processes (in other words, performs detections over and over again) when processing a signal).

Allowable Subject Matter

6. Claim 3-5 and 12-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to further show the state of the art with respect to Apparatus for Reading Data:

    1. U.S. Pat No. 6, 134, 064 to Sato et al., wherein it discloses a sampling clock having a different than a detecting device (Viterbi detector).

    2. U.S. Pat No. 5, 938, 791 to Narahara, wherein it discloses a Viterbi detector that performs maximum likelihood data detection.

    3. U.S. Pat No. 6, 396, 254 to Feyh et al., wherein it discloses a Viterbi detector that performs maximum likelihood data detection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenda P. Rodriguez whose telephone number is 703-305-8411. The examiner can normally be reached on Monday thru Thursday: 7:00-5:00; alternate Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Jeffrey Hofsass can be reached on 703-305-4717. The fax phone numbers

for the organization where this application or proceeding is assigned are 703-308-6743

for regular communications and 703-308-6743 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or

proceeding should be directed to the receptionist whose telephone number is 703-305-

9000.

Richemcnd Dorvil
Primary Examiner

gpr
May 8, 2003